Innovation in the Semiconductor Equipment Industry

(Incremental Innovation vs. Radical Innovation)

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May 2014

BSc Management with Innovation Sustainability & Entrepreneurship

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Abstract

In many organisations, innovation becomes a strategic decision to survive in the world market. Innovation has introduced new technologies or significant systemic changes in many industry areas. When firms need new innovation, the decision requires considerable risk taking such as high or low risk with reasonable benefits. In the most industry, radical and incremental innovations are being used through management practices and technological development. In this paper, we discussed both radical and incremental innovation with an example of semiconductor equipment industry. Semiconductor lithography industry requires the development of innovative technologies when the industry recognises to move to next generation waves. Semiconductor equipment industry has shown fast changes for several decades. In the current industry, semiconductor equipment manufacturers expect to develop radical and incremental changes such as increasing wafer size and shorter wavelength patterning. Leading equipment supplier ASML has developed a new business model by asking its leading customers to co-fund development of a new generation of machines using EUV technology and larger wafer sizes. In this way, customer and supplier share the risks of radical innovation. Threat of radical innovation has prompted ASML’s rivals to seek a defensive merger to protect their market share in the equipment industry. This paper helps to understand how incremental and radical innovation adapts to semiconductor equipment industry.
# Contents

Abstract .......................................................................................................................... 2  
Contents ......................................................................................................................... 3  
List of Tables .................................................................................................................. 5  
List of Figures ................................................................................................................. 6

1. Introduction .................................................................................................................. 7  
  1-1. The Theory of Incremental and Radical Innovation .............................................. 7  
  1-2. The Story of Semiconductor Industry .................................................................. 9  
      (1) Demand for Electronic Chips ........................................................................ 9  
      (2) Changes of Semiconductor Industry with Innovative Technologies .......... 10  
  1-3. Strategies of Semiconductor Industry ................................................................. 12

2. Structures of Lithography Equipment Market ......................................................... 15  
  2-1. Story of ASML ..................................................................................................... 15  
      (1) Corporate History ....................................................................................... 15  
      (2) Semiconductor Lithography Machines of ASML .................................... 16  
      (3) Business Environment of ASML ......................................................... 17  
      (1) Market size and share .............................................................................. 20  
  2-3. Competitors of ASML ....................................................................................... 23  
      (1) Applied Materials Inc. ............................................................................. 23  
      (2) Tokyo Electron Ltd. .................................................................................. 24  
  2-4. Customers of ASML ........................................................................................... 26  
      (1) Current Position of Market ....................................................................... 26  
      (2) Intel Corporation ...................................................................................... 28  
      (3) Samsung Electronics Co., Ltd. ............................................................... 29  
      (4) Taiwan Semiconductor Manufacturing Co. (TSMC) ............................... 31

3. Innovation of Next Generation Semiconductor Industry .......................................... 33  
  3-1. Importance of Increasing Silicon Wafer size .................................................... 33  
      (1) History of Changing Wafer size ................................................................ 33  
      (2) New opportunity of 450mm Wafer ......................................................... 35  
      (3) Economics of 450mm Wafer System ....................................................... 37
3-2. Extreme Ultraviolet (EUV) Technology Development ......................................................... 39
   (1) Development of EUV ...................................................................................................... 39
   (2) Benefits of EUV Technology .......................................................................................... 40
   (3) Challenges of ASML ...................................................................................................... 42
   (4) Expectation of EUV Technology Development ............................................................... 44

4. Management of Innovation at ASML .................................................................................. 46
4-1. Customer Co-Investment Programme (CCIP) ................................................................. 46
4-2. Details of Co-Investors’ Participation .............................................................................. 46
   (1) Intel Corporation ............................................................................................................. 47
   (2) Samsung Electronics Co., Ltd. ....................................................................................... 48
   (3) Taiwan Semiconductor Manufacturing Co. (TSMC) ...................................................... 48

5. Strategic Management of Semiconductor Equipment Industry ........................................ 49
5-1. ASML’s Merger Agreements with Cymer ...................................................................... 49

6. Conclusion ........................................................................................................................ 52
7. References ........................................................................................................................ 54
List of Tables

Table 1. Products of ASML - Wave length & Resolution, and Production throughout per hour

Table 2. Marketing mix of ASML

Table 3. SWOT analysis of ASML

Table 4. Strong Growth Forecast for 2014

Table 5. Top 10 Worldwide Semiconductor Manufacturing Equipment Vendors by Revenue Estimates

Table 6. Top 20 Semiconductor Sales Leaders

Table 7. Semiconductor Capital Spending Outlook - 2013F

Table 8. Market Share in Memory Semiconductor (2010, 4th Q)

Table 9. TSMC Achievements

Table 10. Standard diameters of silicon wafers

Table 11. Installed Capacity Leaders per Wafer Size as of Dec-2013

Table 12. Optical verse EUV lithography

Table 13. The amount of Customer Co-Investment Programme (CCIP)

Table 14. Changes of semiconductor equipment market
List of Figures

Figure 1. Semiconductor end-use markets by application 1994-2004

Figure 2. MOSFET, Defect chemistry in silica-based oxides

Figure 3. The basic Process of patterning IC

Figure 4. Investments by focus area – Applied Materials

Figure 5. Tokyo Electron - Main Product

Figure 6. Semiconductor R&D Spending 1995-2012

Figure 7. Intel Manufacturing Technology Road Map

Figure 8. Moore’s Law Effect on DRAM Pricing Trends

Figure 9. Historic and projected semiconductor demand by wafer size

Figure 10. Wafer cost changes

Figure 11. Design challenges for gigascale integration S. Borkar, -2004

Figure 12. Double Exposure (193nm) verse Single Exposure (13.5nm)

Figure 13. Extreme Ultraviolet Lithography

Figure 14. Projected EUV Cost/pixel at Different Resolutions and Throughputs
1. Introduction

It is widely accepted that most industries require an innovation when they faced limits in their technologies or systems in production lines. Innovation is a strategic decision to adapt in changing technologies, competition and its market. Therefore, innovation influences both a firm’s strategic initiatives and organisational structure. Besides, innovation sometimes causes to promote risk taking. Nevertheless, innovation can provide new opportunities to organisations. In the semiconductor photolithography industry, companies have consistently been requiring innovations when the technologies try to move next generation wave. In other words, innovations of semiconductor equipment industry can bring cost-effective and high performance of new technologies. There are two innovations which are incremental and radical innovation. The incremental innovation can be characterised by predictability and reliability with low risk. In contrast, radical innovation usually offers dramatic improvements with disruptive technologies from existing markets. In case of semiconductor industry, increasing silicon wafer size was affected by incremental innovation. On the other hand, the needs of shorter wavelength in photolithography usually seek disruptive technologies which come from radical innovation. The semiconductor equipment industry has the history of significant changes during several decades. When they tried to develop new generation technologies, they have spent a huge amount of R&D costs and time. And then, the previous technology had disappeared by successful development or innovations in marketplace. Following this, next generation technology has brought significant changes with reasonable benefits. In the current industry, the semiconductor equipment manufacturers expect to develop next generation wave with incremental and radical changes. Consequently, we will discuss how incremental and radical innovations adapt to the photolithography industry. Before discussing innovations of semiconductor equipment industry, this chapter will introduce theories of incremental and radical innovation, then, the story of semiconductor industry will help to understand for strategies of the semiconductor equipment industry.

1-1. The Theory of Incremental and Radical Innovation

Incremental innovation can be defined as improvements or refinements of existing technologies and process (Banbury & Mitchel, 1995). Radical innovation was defined by Kobeg et al. (2003) as strategic change in products / services, markets served, and technological breakthroughs used to produce a product based in significant innovation. In other words, incremental and radical innovation requires different management approach and different sets of competences.

In details, incremental innovation is critical to keep companies competitive with existing technologies and process (Utterback, 1994). Even though, incremental innovation has less potential for returns for
the organisation, the associated risks are much less than radical innovation. Moreover, it needs smaller
endeavours with using fewer resources. Therefore, incremental innovation can be explained as to be
continuous in the few areas in product or process innovation where future improvements can be
expected. For example, increasing television and mobile screen size often lead to small changes in
growth. It was stated by Dosi (1982) that incremental innovation can lead to a significant
improvement in price or functionality. It can be relatively advantageous to reproduce the technology.
Nonetheless, it might be extremely difficult to replicate intangible asset and to replicate know how
such as experience, routine and culture of the innovator. For this reason, Freeman (1982) explained
that market leaders who frequently introduce or adopt important incremental innovations, tend to
maintain or even improve their market share. Consequently, the drivers of incremental innovation
may have approaches to continuous improvement such as total quality management, lean
manufacturing and world-class manufacturing.

On the other hand, Utterback (1994) explained that radical innovation has threats to transform the
industry itself by destroying the existing markets with disruptive technologies, thus creating the next
great wave. Moreover, radical innovation may bring dramatic benefits for an organisation through
increasing sales and extraordinary profits. It was stated by Schumpeter (1942) that radical innovation
makes the difference between life and death for market anticipants. In other words, it would bring the
disappearance of both individual firms and whole industry. Nelson and Winter (1982) added that
industry transformation happens also because adoption of radical innovation makes old routines
obsolete and that the development of new routines is costly and lengthy process. Besides, radical
innovation is not easy to obtain, because it usually requires large amount of investment on R&D with
a highly uncertain return on investment. Nevertheless, radical innovation can be the first mover in the
market. As a first-mover, a company can monopolise the market and the related profits, as, for a
certain period of time, it is the only player in a particular market (Nelson and Winter, 1982).
Therefore, first mover with market dominance would create a competitive advantage through barrier
to entry. However, if radical innovation has adopted successfully in the market, imitator may appear
with free ride on first movers’ innovation. This is because of R&D costs are high and market would
completely new. According to Scherer (1980), imitator may learn a lot from imitating and may
become first-movers in the next phase of technological development. Consequently, if first mover
cannot keep improving the existing product, later adopter would try to change customers’ preferences
in the market.

It can be deduced that incremental and radical innovation has both advantages and disadvantages.
Even though, radical innovation has the advantage of creating a step change in growth, it would bring
the high level of risk and high cost of failure. In contrast, incremental innovation has lower risk and
the possibility of achieving small degrees of growth. However, it would be slower to reach growth targets than other competitors. It means that companies may lose their competitive advantage in the market. It is widely accepted that most organisations seek a dual approach to the size and scope of their innovation. In other words, they try to develop some potentially radical innovations which can bring significant strengths in the medium to long term. As a result, decision making of innovation process has become more complex with risk taking in order to fund the innovation.

1-2. The story of semiconductor industry

(1) Demands for Electronic Chips

It is clear that the development of Integrated Circuit (IC) has changed the trend of global electronics industry. In “electronics components” manufacturing industry, there is small growth in the international share of R&D investment between 1985 and 2001. In addition, the market for semiconductor components was dominated by Personal Computer (PC) which sought to be made smaller and more cost-efficient in the market. After that, the demand for semiconductor components in PC industry was declined by changing in consumption pattern such as wireless communications and other non-PC consumer products. Moreover, it also affected to change importance of implications for the geographic location of demand for semiconductor components.

![Semiconductor end-use markets by application 1994-2004](image)

Figure 1. “Semiconductor end-use markets by application 1994-2004”, Source: Integrated circuit Engineering (ICE) and IC Insights.
According to Ernst (2005), Producers of electronic systems sometimes required that functionally be based on features in the semiconductor components incorporated in the products – so-called system-on-chip designs that are more complex and required more intensive interaction between system and chip designers. In other words, it is possible to say that the number of new application by using the technique of photolithography has been increased significantly. Furthermore, increasing the needs of system providers required more flexible size than one-size-fits for semiconductor components. Therefore, close interaction was needed between producers and designers of components for heterogeneous electronic system. After that, semiconductor equipment manufacturers have focused on lower production costs of electronic chips with the economies of scales. However, it required a huge capital investment that would bring lower unit costs through producing large volumes of semiconductor components. At the same time, the design cycle of new semiconductor products represented shorter and uncertain product life cycle. As a result, it caused the risk of investment on a fabrication facility in photolithography industry.

During the 1990s, the number of technology development alliances among U.S. had declined in the global semiconductor industry. Following this, European, Japanese, Taiwanese and Korean electronic chip manufacturers experienced fast growth in the global market. For example, Southeast Asian countries has shown constantly growing share of global semiconductor industry activities. Furthermore, its expansion of semiconductor manufacturing industry has brought innovations-related activities within the global semiconductor equipment industry such as increasing wafer size and new technology of fabrication.

(2) Changes of Semiconductor Industry with Innovative Technologies

The first practical electron tube called the ‘Fleming Valve’ was invented by John Ambrose Fleming in 1904. The Fleming valve was known today as a diode. The “oscillation valve” was based on “Edison effect” that converted alternating radio signal currents into direct currents. In 1921, the first magnetron electronic vacuum tube was invented by Albert W. Hull. The magnetron took the form of a coaxial cylindrical anode and cathode with an axial magnetic field produced by an external coil. After that, it used for the tube scanning system of television. Following this, Hull and Williams co-invented the ‘tetrode’ electronic vacuum tube in 1926. Consequently, its incremental changes had brought new concepts of transistor in this industry. Then, technological limitations of electronic vacuum tube affected that many technicians sought to develop new technologies such as the Point-Contract-Transistor, the Junction Transistor. Indeed, silicon material based transistor technologies were introduced rapidly after the Second World War.

With respect to Metal Oxide Semiconductors (MOS), in 1959 M. M. (John) Atalla and Dawon Kahng at Bell Labs invented the first successful insulated-gate field-effect transistor (FET) which had been
achieved by overcoming the "surface states" that blocked electric fields from penetrating into the semiconductor material (World Scientific Publishing, 1991). Investigating thermally grown silicon-dioxide layers, it could be mainly declined at the interface between the silicon and oxide in a sandwich comprising layers of metal (M - gate), oxide (O - insulation), and silicon (S – semiconductor). For a profitable business, the entrepreneurs of semiconductor industry needed to build reproducible and economical MOS manufacturing processes. During this time, memory circuit had used in one of its main frame computer by IBM who expected the rapid price declines of semiconductor devices.

In the late 1960s, Moore and Noyce established San Francisco Peninsula powerhouse: Intel. They planned to produce large scale integrations (LSI) memory circuits which were made possible the storage of a large number of memory bits with thousands of transistors. Fairchild Semiconductor had developed the production techniques to manufacture theses circuits.

In 1965, Gordon Moore (Fairchild Semiconductor’s Director of R&D) published an internal paper which includes the number of components per integrated circuit for minimum cost per component. In addition, he predicted “the development of integrated electronics for perhaps the next ten years.” In other words, Gordon Moore believed that the number of components per chip would increase a doubling every 18 months. Thus, the performance of electronic chip would be doubled during same period. This is also known as “Moore’s Law”. At the 1975 IEEE (International Electron Devices Meeting), Moore noted that the future rate of increase would be slowed to “a doubling every two years” by complexity of photolithography, wafer size and process technology. This prediction became the basic principle of the semiconductor industry. Therefore, technologists have been challenging the delivery annual breakthroughs with “Moore’s Law”.

The first commercial MOS circuit was called the 1101 which was a 256-bit static random-access memory (SRAM) chip. However, it showed too slow and too costly for computers (Sideris, 1973). Following this, Intel developed a more integrated product, the 1103 which was a dynamic random-
access memory (DRAM). By this development, it had been used for future version of its main frame computer by Honeywell. Furthermore, it was rated a 512-bit DRAM among semiconductor suppliers. After that, Intel designed new 1,024-bit circuit by requesting from Honeywell’s engineers. The 1103 was markedly received in the electronic chip market. As a result, it boosted Intel’s sales which had sold $500,000 worth in 1969, had $4 million in revenues the following year. Consequently, Intel could have a clear leadership in the semiconductor industry.

In 1970 and 1971, the US economy faced a severe economic recession; therefore, Richard Nixon administration carried forward restrictive monetary policy. For this reason, the demand for micro circuit had also declined in the market. This downturn was affected by a significant decline in the demand for semiconductor components in the military/aerospace sector and the computer industry. However, changes in consumer electronics brought increasing demands for integrated circuits. For example, manufacturers of radios, stereos, and televisions had started using microcircuits from 1972. At the same time, the demand for semiconductor memories boomed in the market. Intel had established itself as the main producer of semiconductor memories for 1103 DRAM which was the main beneficiary product. And then, Intel organised high-volume production for growing market demand. It required a massive training program and built new wafer-fabricating facilities. In addition, they developed 3-inch wafers from a 2-inch wafer. In other words, a 3-inch wafer could make more than twice output of memory chips and microprocessors in the same manufacturing space. As a result, Intel reached 80 per cent share of the 1103 market with 3-inch wafers.

1-3. Strategies in Semiconductor Industry

By the electronic infrastructure, the rules of electronic market have been changing such as global competition intensifies, technology accelerates and product life cycles shorten. The ever-growing demand for technological electronics devices and gadgets has affected to increase manufacturing capacities of electronic chip manufacturers. Besides, lower production cost of electronic chips was required for price competitiveness in the market. In other words, the profitability of firms depends on lower manufacturing cost in the semiconductor industry. For example, each company seeks to maintain high profit margin through cost effective strategies. Moreover, an increase of investment on R&D has focused on sufficient capital outlays for future generations of devices. Following this, the aims of semiconductor equipment industry was not only increasing wafer size but also improving photolithography technologies.

A silicon wafer is a thin slice of silicon crystal which is available in various sizes for different applications through specialised way. Electronic chips can be made by the fabrication of integrated
circuits (ICs) on the silicon wafer. Therefore, the silicon market has been expanding constantly by semiconductor manufacturers. In the electronic chip manufacturing, the most important task is lower production cost of electronic chips per wafer. In fact, average production cost per wafer has been increased by more than three times over the last decades. Nonetheless, the real cost of manufacturing semiconductor chips has decreased continually, even if the cost of labour, material and capital expenditure has grown in the production. This is because of the number of transistor per wafer has increased faster than its manufacturing cost. In other words, larger wafer size contributes to improve profitability through increasing the productivity of fabrication equipment and operations. Therefore, most companies focus on the economies of scale through expanding wafer size in their production.

The origin of lithography is followed by a description of photolithography which technique transfers copies of a master pattern onto the surface of a silicon wafer. For example, lithography transforms complex circuit diagram into pattern through a succession of exposure and processing steps to form a number of superimposed layers of insulator, conductor and semiconductor materials. Moreover, there are 8-25 lithography steps with several hundred processing steps between exposures for the fabrication of a packed IC. For these reasons, photolithography is the most expensive, complicated and critical process of modern IC manufacturing. In the industry of semiconductor integrated circuits (ICs), lithography is even more critical than other technologies because it can bring to going smaller pattern, higher speed and much less energy consumed per computing function.

For patterning of ICs, it takes place on the wafer in two steps. (Pease and Chou, 2008)

1) Lithography, the patterning of a resist film on top of the functional material
2) Transferring the resist pattern into the functional material; and usually by etching.

(First make mask and then project the mask pattern onto a resist-coated wafer)

Figure 3. “The basic Process of patterning IC”, Source: Chris (www. Lithoguru.com)

The complex structures of ICs make up a transistor and the many wires that connect the millions of transistors of a circuit. Therefore, a lithography process is significant relate to IC’s performance. In the semiconductor equipment industry, photolithography showed the technical limitation for further
advances in feature size reduction and transistor speed. According to Pease and Chou (2008), ICs will continue to be manufactured until at least the “22nm node (the line width of an equal line-space pattern)”. Nevertheless, optical lithography may not be the most economical below 22nm ranges because nanometre-scale printing can be a difficult challenge. Recently, extreme ultraviolet (EUV) and electron beam lithography (less than 10nm wide mask making) have been developing in the industry. Even though, the nanometre-scale printing of optical lithography has great risk, emerging new technologies of lithography will change the trend of semiconductor industry.

During the past few decades, the semiconductor industry was mainly based on Moore’s Law with incremental changes. However, many companies faced the limitation of 300 mm wafer in their production line. In other words, the semiconductor market is still seeking the development of low production costs and high performance electronic chip such as bigger wafer size and shorter wave lengths. In the current semiconductor industry, it desires to accept new technological trajectory. Dosi (1982) stated that new ideas, technologies, equipments and materials would be main factors of future technological innovation. Furthermore, he added that if the possibility is high that technological trajectories will develop under a specific technological paradigm, the incentive to look for other technological paradigms decreases. For example, it is widely accepted that EUV technology requires high costs, however; it can show new technological innovation as a trajectory disruptive and radical innovation.
2. Structure of Lithography Equipment Market

For manufacturing electronic chips, manufacturers need to have both photolithography machine and silicon wafers. In the current semiconductor equipment industry, there are three large companies such as ASML, Applied Materials and Tokyo Electron. In other words, Applied Materials and Tokyo Electron are the largest competitors of ASML in the semiconductor equipment market. In recent year, ASML decided to develop disruptive technologies for shorter wavelength lithography technology which is called Extreme Ultraviolet Lithography (EUVL) This technology requires huge investment of R&D that means their radical changes involve the high level of risk and high cost of failure. Nevertheless, their decision can be seen as positive, because, ASML has large customers such as Intel, TSMC and Samsung who agreed to invest in the development of EUVL and 450mm wafer system through ASML’s Customer Co-Investment Programme (CCIP). This part will introduce information of the semiconductor equipment market including ASML, Applied Materials and Tokyo Electron. Furthermore, the part of ASML’s large customers will support to understand the structure of semiconductor manufacturing market.

2-1. Story of ASML

(1) Corporate History

According to ASML official website, ASML was founded in 1984, and they are one of the largest companies in the manufacture of advanced technology systems for the semiconductor equipment industry. The company was started by 50/50 joint venture between Philips and Advanced Semiconductor Materials International in Eindhoven. In 1985, new headquarters opened in Veldhoven, as well as the North American headquarters in Arizona and Tempe. However, ASMI withdrew from the ASML joint venture. And then, the production capacity had grown to around 200 chip manufacturing machine per year. As a result, the company became the third largest manufacturer in the world in 1990. Four years later the joint venture partner Philips sold most of its shares to public. In 1995, ASML’s initial public offering was launched at Amsterdam and NASDAQ stock exchanges. For supporting chip manufacturers in Asia, ASML opened an office in South Korea. One year later ASML entered to the top 10 electronic chip manufacturing equipment manufacturers in the world. In 2000, ASML became the biggest manufacturer with a member of the Silicon Valley Group (SVG). In 2006, ASML became a world market leader in photolithography industry; moreover, the company increased significantly to invest in research and development. ASML is committed to provide leading edge technologies to their customer that is production-ready at the earliest possible date (Tilburg, 2007). In other words, ASML technologies provide process solutions; sustain a competitive edge and
enabling customers to gain in the market place. In 2009, the financial crisis caused to shrink the world economy as well as the semiconductor industry. Therefore, the company needed to cut costs, nonetheless, they maintained strategic spending for research & development which helped to protect technology leadership in marketplace. Even though, the economic recession dropped significantly in revenue, the demand for electronic chips was increased by gadgets’ innovations such as smartphones and tablet PCs. In 2010, ASML moved to boost their production capacity for market demands. Since 2011, next generation technology of ASML has introduced to electronic chip manufacturers. The technology is known as Extreme-Ultra-Violet-Lithography (EUVL). At present ASML has been accelerating the development of next- generation lithography technologies. For developing new technology, ASML introduced the customer Customers Co-investment Programme (CCIP) with their large customers such as Intel, Samsung and TSMC. In this programme, customers decided to invest 1.38 billion euros to ASML’s research and development of next-generation lithography technologies over five years (ASML, 2014). As a result, the corporate performance ASML brought to receive various awards for customer satisfaction and for cost of ownership and technology leadership.

(2) Semiconductor Lithography Machines of ASML

<table>
<thead>
<tr>
<th>PAS 5500 Series</th>
<th>Wave Length</th>
<th>Resolution</th>
<th>Production Throughout (Wafer, Per hour/ Shots)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100D</td>
<td>365 nm</td>
<td>0.40 μm</td>
<td>150-mm 40 shots: 200-mm 70 shots:</td>
</tr>
<tr>
<td>275D</td>
<td>365 nm</td>
<td>0.28 μm</td>
<td>150-mm 40 shots: 200-mm 70 shots:</td>
</tr>
<tr>
<td>350C</td>
<td>248 nm</td>
<td>0.15 μm</td>
<td>150-mm 40 shots: 200-mm 70 shots:</td>
</tr>
<tr>
<td>750F</td>
<td>248 nm</td>
<td>130 nm</td>
<td>200-mm 46 shots:</td>
</tr>
<tr>
<td>850D</td>
<td>248 nm</td>
<td>110 nm</td>
<td>200-mm 46 shots:</td>
</tr>
<tr>
<td>1150C</td>
<td>193 nm</td>
<td>90 nm</td>
<td>200-mm 46 shots:</td>
</tr>
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</table>

<table>
<thead>
<tr>
<th>TWINSCAN XT Series</th>
<th>Wave Length</th>
<th>Resolution</th>
<th>Production Throughout</th>
</tr>
</thead>
<tbody>
<tr>
<td>XT/400K</td>
<td>365 nm</td>
<td>350 nm</td>
<td>300-mm 96 shots</td>
</tr>
<tr>
<td>XT/800K</td>
<td>248 nm</td>
<td>120 nm</td>
<td>300-mm 96 shots</td>
</tr>
<tr>
<td>XT/850K</td>
<td>248 nm</td>
<td>110 nm</td>
<td>300-mm 96 shots</td>
</tr>
<tr>
<td>XT/1000K</td>
<td>248 nm</td>
<td>80 nm</td>
<td>300-mm 125 shots</td>
</tr>
<tr>
<td>XT/1450H</td>
<td>193 nm</td>
<td>65 nm</td>
<td>300-mm 125 shots</td>
</tr>
<tr>
<td>XT/1950Hi</td>
<td>193 nm</td>
<td>38 nm</td>
<td>300-mm 125 shots</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>TWINSCAN NXT Series</th>
<th>Wave Length</th>
<th>Resolution</th>
<th>Production Throughout</th>
</tr>
</thead>
<tbody>
<tr>
<td>NXT:1960Bi</td>
<td>193 nm</td>
<td>38 nm (single exposure)</td>
<td>300 mm 96 shots:</td>
</tr>
<tr>
<td>NXT:1970Ci</td>
<td>193 nm</td>
<td>38 nm (single exposure)</td>
<td>300 mm 96 shots:</td>
</tr>
<tr>
<td>TWINSCAN NXE Series</td>
<td>Wave Length</td>
<td>Resolution</td>
<td>Production Throughout</td>
</tr>
<tr>
<td>---------------------</td>
<td>-------------</td>
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<td>-----------------------</td>
</tr>
<tr>
<td>NXE:3300B (EUV)</td>
<td>13.5 nm (EUV)</td>
<td>22 nm</td>
<td>300-mm 69 shots:??</td>
</tr>
</tbody>
</table>

Table 1. “Products of ASML - Wave length & Resolution, and Production throughout per hour”, Source: ASML (2014)

The technological challenges of ASML have brought advanced products which become shorter wavelength, resolution and faster production-throughout. In the early stage, photolithography machine of ASML used 365 nm wave-lengths with 0.40 μm resolution. Moreover, the capacity of its machine was 70 shots per hour. In recent year, ASML has released NXE: 3300B which used 13.5nm EUV light with 69 wafers production throughout per hours. According to ASML (2012), a high maximum wafer scanning speed allows optimal use of the source intensity over the largest possible range of resist sensitivities and exposure doses. Therefore, it brought to maximise throughput. At present ASML received 11 orders for NXE: 3300B (ASML official website).

(3) Business Environment of ASML

During the past 30 years, the global semiconductor industry has been changed by rapid rates of technological changes, rising costs for production capacity and declining prices. In this industry, incremental and radical changes are always required to develop new generation electronic chip manufacturing. Therefore, ASML is also affected by changing the market trends such as lower production cost, declining price and the demand for disruptive technologies. Thus, the company needs to move sensitively with both managerial skills and technology development.

In the manufacturing department and logistics, the supply chain consists of all the suppliers who are very important in the all manufacturing processes. Therefore, the manufacturing department of ASML seeks just in time management. In addition, AMSL develops their new product together with their customers who recognise the importance of new machines and techniques. The business support department covers the development of new machine and the quality control and good working order of the machines. Moreover, ASML has informal culture in the management. The work environment and production is influenced positively by communication and cooperation between parties. This structure brought the mission of ASML for being a leading and innovative company.
The product is actually the only aspect of the marketing mix which is really concentrated on. The technology research for innovation and improvement of the lithography systems has very high priority at ASML.

The price is not an actual marketing tool, because there are few competitors and ASML does not compete with them through price, but through advancing and innovating their systems.

The headquarters of ASML is located in Veldhoven, but there is an ASML office near every customer. ASML is committed to provide a good service for its customers and this way ASML maintenance can be at location of the customer without delay.

Promotion is not needed, because it is well known by the customers and potential customers what ASML has to offer, because it is communicated in meetings throughout the whole designing process.

<table>
<thead>
<tr>
<th><strong>Marketing mix</strong></th>
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<tbody>
<tr>
<td><strong>Product</strong></td>
<td>The product is actually the only aspect of the marketing mix which is really concentrated on. The technology research for innovation and improvement of the lithography systems has very high priority at ASML.</td>
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</tr>
<tr>
<td><strong>Place</strong></td>
<td>The headquarters of ASML is located in Veldhoven, but there is an ASML office near every customer. ASML is committed to provide a good service for its customers and this way ASML maintenance can be at location of the customer without delay.</td>
</tr>
<tr>
<td><strong>Promotion</strong></td>
<td>Promotion is not needed, because it is well known by the customers and potential customers what ASML has to offer, because it is communicated in meetings throughout the whole designing process.</td>
</tr>
</tbody>
</table>

Table 2. “Marketing mix of ASML”, Source: University of Applied Sciences (2009)

The main strategy of ASML is the customer focus. They usually serve different types of chipmakers with premium value for their customers on the semiconductor equipment market. Moreover, ASML provides all maintenance of the twin-scans to their clients. The semiconductor equipment industry is a million dollar industry, therefore; it is essential that customer supports usually have to be provided within 24 hours. In addition, strategic investments in research and development brought a leading position with their new technologies for manufacturing chips in the market. It is clear that many companies tried to cut their investments in research and development by the recent global economic crisis caused. In contrast, ASML continued the investments in R&D during same period. The operational excellence is another key strategic point. For example, ASML outsourced various components and subassemblies of the products. Hereby, the cooperation with suppliers improves quality and logistics technology as well as declining cost. Furthermore, a flexible labour model reinforces the ability to adapt quickly to the market cycles. As a result, the risk of falling out minimised by more than 25 per cent in downturn.
## SWOT Analysis

<table>
<thead>
<tr>
<th>Internal</th>
<th>Positive</th>
<th>Negative</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td><strong>Strengths</strong></td>
<td><strong>Weaknesses</strong></td>
</tr>
<tr>
<td></td>
<td>- Fast and exact twin-scans</td>
<td>- High costs</td>
</tr>
<tr>
<td></td>
<td>- Enthusiastic employees</td>
<td>- Limited number of system produce, due limited number of suppliers</td>
</tr>
<tr>
<td></td>
<td>- Good and fast customer support</td>
<td>- High percentage of net sales from few customers with a small number of products</td>
</tr>
<tr>
<td></td>
<td>- Establishment worldwide</td>
<td>- Success in future dependent on attraction and retain sufficient educated employees</td>
</tr>
<tr>
<td></td>
<td>- Short time of delivery</td>
<td></td>
</tr>
<tr>
<td></td>
<td>- R&amp;D investments</td>
<td></td>
</tr>
<tr>
<td></td>
<td>- Innovative</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>External</th>
<th>Opportunities</th>
<th>Threats</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>- Independent suppliers</td>
<td>- Source of new technology (Moore’s law)</td>
</tr>
</tbody>
</table>

With respect to SWOT analysis, new technology is not infinite. Therefore, a large opportunity is the investment in R&D with the source of new technology. In other words, there can be acquired more and new technologies to work near the boundaries when large investments are made in R&D. And then, the fast and exact twins-scans with the intense competition would be another opportunity. ASML is capable of producing semiconductor equipment which can produce chips fast and exact. On the other hand, the ability of attracting and retain sufficient educated employees can be a large threat in the future. For example, skilled and well educated employees will be key resources for research in the source of new technology. Thus, if ASML does not have sufficient educated and skilled employees, they cannot be able to make progress in the lithography technology. Following this, the intense competition will be large threat that is the high percentage of net sales from few customers with a small number of products. Consequently, loosing clients can be explained as a significant impact on ASML because a high percentage of their revenues usually come from a small number of clients.

Table 3. “SWOT analysis of ASML”, Source: University of Applied Sciences (2009)
2-2. Market Competition of Semiconductor Equipment Market

(1) Market size and share

According to Semiconductor Equipment and materials International (SEMI), the amount of order for new equipment increased from 2013, even if its amount is below 2012 levels. The recently published SEMI Year-end Forecast predicts that the new equipment market will improve by 23.2 percent (to $39.46 billion) for 2014. Besides, Taiwan, South Korea and North America will keep spending for new wafer processing equipment. For example, new spending plans have been announced by many companies such as TSMC, Samsung, Intel, SK Hynix, Global foundries, UMC, and for some Japanese facilities and LED facilities. In other words, a few companies can afford the rising costs for R&D and upgrading facilities for the leading edge technologies. New spending plans will expect for 17nm and below node.

In addition, the semiconductor equipment market expects the effect of developing 450mm wafer and EUV technology. For instance, the development of 450mm wafer system affects to improve productivity of fab equipment with economies of scale production. However, the successful use of EUV light can create the most efficient and cost-efficient power source for the next generation of high performance chip production. In consequence, the market trend of semiconductor industry will be changed by introduction of both technologies in marketplace.


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For 2012, worldwide semiconductor capital equipment spending had declined by 16.1% from 2011. Wafer-level manufacturing underperformed because it was pulled down by weakness in photolithography and deposition in 2012. For example, a significant decrease of memory manufacturing-related purchases was impacted by slowing overall semiconductor device demand in the second half of 2012. Thus, it caused to decline manufacturing equipment sales.

In details, Applied Materials (AMAT) was back to the top position by increasing share of the Wafer Front End (WFE). However, it seemed entirely due to the Varian Semiconductor Equipment Associates acquisition. In fact, Applied Materials’ share of WFE continued to decline excluding mergers and acquisitions. Therefore, it can be seen that Applied Materials had lost their market share in process control (metrology and inspection) and Chemical Mechanical Planarization (CMP).

The growth rate of ASML has reduced by 28% in 2012. It affected to descend from market leader to second position in marketplace. For instance, semiconductor equipment market recognised weakness in photolithography and limited sales in extreme ultraviolet (EUV) machine. Nevertheless, ASML is
well positioned in the market because the price of extreme ultraviolet (EUV) lithography equipment is approaching $100 million each.

Even though, Tokyo Electron Ltd showed a decrease of their growth rate by 17.2%, they were well positioned in semiconductor equipment market. According to Gartner (2014), Tokyo Electron Ltd. (TEL) benefited from its relative strength in the non-lithography sectors it serves.

2-3. Competitors of ASML

(1) Applied Materials Inc.

According to Applied Materials official website, Applied Materials was founded in 1967 with seed money from local investors. Nowadays, Applied Materials has become the global leader in nanomanufacturing technology solutions with a broad portfolio of innovative equipment, service and software products for the fabrication of semiconductor chips, flat panel displays, solar photovoltaic cells, flexible electronics and energy efficient glass. In the early years of the semiconductor equipment industry, manufacturers usually built their own equipment. However, original engineering team of Applied Materials changed fabrication systems with the first chemical vapour deposition (CVD) reactor which is known as the AMV 300. During same period, they sought to expand globally. In 1975, Applied Materials had serious financial problems by a severe recession of the entire semiconductor industry. Following this, a new president, James C. Morgan decided to stop producing several unprofitable products, then, they focused exclusively on the semiconductor equipment industry. In 1987, Applied Materials introduced the Precision 5000 CVD which was a new revolutionary system including featured single-wafer and multi-chamber. Especially, this system supported to handle the new larger and more complex microchips.

Consequently, the company became the undisputed leader in single-wafer, multi-chamber fabrication architectures. In the 1990s, the company showed further product expansion, including a move to supply flat panel display equipment. By the late 1990s, the semiconductor industry focused mainly on a triple wave of challenges such as shrinking transistor size, a shift to larger wafers and the introduction of new materials. Applied Materials engineers adapted quickly to the new market trends. Thus, the company was the first semiconductor equipment supplier for 300mm production systems. And then, significant operational improvements have brought a positive financial results and to gain market share with its technology portfolio and new products. In addition, the company invests on solar cells that will more clean power in the near future.

Applied Materials provides system that perform the most of the primary processes used in chip fabrication such as atomic layer deposition (ALD), chemical vapour deposition (CVD), physical vapor deposition (PVD), electrochemical deposition (ECD), rapid thermal processing (RTP), chemical
mechanical planarization (CMP), wet cleaning, and wafer metrology and inspection (Applied Materials, 2011). Moreover, semiconductor manufacturing systems are utilised by integrated device manufacturers and foundries to build and package memory and logic. Semiconductor equipment of Applied Materials delivers single-wafer systems with multiple process chambers. For example, each wafer can be processed separately in its own environment. It is clear that the semiconductor industry have been following to increasingly larger wafers to build chips. Therefore, 300 mm or 12-inch, wafers is widely accepted the largest volume production of advanced chips. Furthermore, the company also offers earlier-generation 200mm wafer systems. Applied Materials has invested significantly in research, development and engineering (RD&E). As a result, the company can deliver new products and technologies to meet long-term growth strategy. In 2011, Applied Materials developed new logic and memory chip technologies by using below the 22nm node. At present the company focused continually on optimizing the cost-effectiveness of TSV technologies. TSV is an emerging solution for interconnecting three dimensional chip stacks to provide better device performance, lower power consumption and the integration of heterogeneous devices (Applied Materials, 2011). Furthermore, the company also allocates a strategic investment in order to develop new products such as 450mm wafer systems.

![Investments by Focus Area](image)

**Figure 4. “Investments by focus area – Applied Materials”, Source: Applied Ventures (2010)**

(2) Tokyo Electron Ltd.

Tokyo Electron is one of world-leading suppliers in semiconductor production equipment (SPE) and flat panel display (FPD) production equipment industry (Tokyo Electron official website). The company offers a broad line-up of products that shows superior process performance and high productivity to semiconductor manufacturers. Therefore, their competitive strength provides real
customer needs and responds to them with cutting-edge technology and products. Tokyo Electron has a global network including Japan, the U.S., Europe and Asia that is available to provide digital networks by contributing technology innovation. In 2012, the economic environment surrounding Japan had experienced increasingly severe and even chaotic conditions. Nevertheless, the demand for mobile devices has been expanding such as smartphones and tablets. For this reason, IT device manufactures require even higher performing semiconductors than before. And then, the manufacture of logic chips needs to meet lower power consumption and higher telecommunication standards. The company will provide technological innovation in semiconductor production equipment (SPE) for their customers’ demand.

It is clear that semiconductor equipment is the key components of digital products. Tokyo Electron has released a wide range of equipment for superior technical supports and services. These products can be divided by six groups such as coaters and developers, plasma etch systems, thermal processing systems, single wafer deposition systems, cleaning systems used in wafer processes, and wafer probers used in the wafer testing process (Tokyo Electron, 2012). In recent year, the company has expanded the products for advanced packaging processes, including equipment used for through-silicon via (TSV) processes. Therefore, Tokyo Electron will continue to drive semiconductor capital investment for the comprehensive strengthening of existing products, the launching of new businesses to link these market and technology trends to business expansion (Tokyo Electron, 2012). For example, the served available market (SAM) will be developed continually for increasing sales of single wafer deposition systems.

![Image](https://example.com/image.png)

Figure 5. “Tokyo Electron - Main Product”, Source: Tokyo Electron (2010)

According to Tokyo Electron Annual Report (2012), the company predicted the semiconductor industry will not be limited to computers and telecommunications but will expand to healthcare,
agriculture and myriad other applications. Furthermore, the speed of electronic chips will play an important role in achieving technology development. Thus, the development of cutting-edge technology requires more investment the integration of expert knowledge in a variety of fields to invent entirely new technical concepts. For instance, semiconductor manufacturers are struggling to develop spin transfer torque-magneto-resistive random access memory (STT-MRAM) which technology will operate using less than half the energy consumed for DRAM and SRAM devices. It is true that Tokyo Electron has introduced advanced technologies such as miniaturisation, vacuum, plasma, thermal processing, coating developing, cleaning, wafer-transfer and clean technologies. Furthermore, the company has successfully taken a high market share in each of the product fields with high profit margin. However, delays in the launch of new products can affect the future business performance.

2-4. Customers of ASML

(1) Current Position of Market

<table>
<thead>
<tr>
<th>1Q13 Rank</th>
<th>1Q12 Rank</th>
<th>Company</th>
<th>Headquarters</th>
<th>1Q12 Total Semi</th>
<th>1Q13 Total Semi</th>
<th>2012/2011 % Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>Intel</td>
<td>U.S</td>
<td>11,874</td>
<td>11,555</td>
<td>-3%</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>Samsung</td>
<td>South Korea</td>
<td>7,067</td>
<td>7,952</td>
<td>13%</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>TSMC*</td>
<td>Taiwan</td>
<td>3,526</td>
<td>4,460</td>
<td>26%</td>
</tr>
<tr>
<td>4</td>
<td>5</td>
<td>Qualcomm**</td>
<td>U.S</td>
<td>3,059</td>
<td>3,916</td>
<td>28%</td>
</tr>
<tr>
<td>5</td>
<td>4</td>
<td>Toshiba</td>
<td>Japan</td>
<td>3,255</td>
<td>2,938</td>
<td>-10%</td>
</tr>
<tr>
<td>6</td>
<td>6</td>
<td>TI</td>
<td>U.S</td>
<td>2,934</td>
<td>2,718</td>
<td>-7%</td>
</tr>
<tr>
<td>7</td>
<td>8</td>
<td>SK Hynix</td>
<td>South Korea</td>
<td>2,115</td>
<td>2,577</td>
<td>22%</td>
</tr>
<tr>
<td>8</td>
<td>9</td>
<td>Micron</td>
<td>U.S</td>
<td>2,102</td>
<td>2,185</td>
<td>4%</td>
</tr>
<tr>
<td>9</td>
<td>10</td>
<td>ST</td>
<td>Europe</td>
<td>1,999</td>
<td>1,977</td>
<td>-1%</td>
</tr>
<tr>
<td>10</td>
<td>11</td>
<td>Broadcom**</td>
<td>U.S</td>
<td>1,770</td>
<td>1,954</td>
<td>10%</td>
</tr>
<tr>
<td>11</td>
<td>7</td>
<td>Renesas</td>
<td>Japan</td>
<td>2,363</td>
<td>1,886</td>
<td>-20%</td>
</tr>
<tr>
<td>12</td>
<td>16</td>
<td>Global Foundries*</td>
<td>U.S</td>
<td>1,170</td>
<td>1,240</td>
<td>6%</td>
</tr>
<tr>
<td>13</td>
<td>14</td>
<td>Infineon</td>
<td>Europe</td>
<td>1,292</td>
<td>1,212</td>
<td>-6%</td>
</tr>
<tr>
<td>14</td>
<td>12</td>
<td>AMD**</td>
<td>U.S</td>
<td>1,585</td>
<td>1,088</td>
<td>-31%</td>
</tr>
<tr>
<td>15</td>
<td>17</td>
<td>NXP</td>
<td>Europe</td>
<td>969</td>
<td>1,085</td>
<td>12%</td>
</tr>
<tr>
<td>16</td>
<td>13</td>
<td>SONY</td>
<td>Japan</td>
<td>1,514</td>
<td>1,049</td>
<td>-31%</td>
</tr>
<tr>
<td>17</td>
<td>18</td>
<td>NVidia**</td>
<td>U.S</td>
<td>935</td>
<td>1,006</td>
<td>8%</td>
</tr>
<tr>
<td>18</td>
<td>19</td>
<td>Free scale</td>
<td>U.S</td>
<td>910</td>
<td>917</td>
<td>1%</td>
</tr>
<tr>
<td>19</td>
<td>20</td>
<td>UMC*</td>
<td>Taiwan</td>
<td>804</td>
<td>898</td>
<td>12%</td>
</tr>
<tr>
<td>20</td>
<td>15</td>
<td>Fujitsu</td>
<td>Japan</td>
<td>1,216</td>
<td>894</td>
<td>-26%</td>
</tr>
</tbody>
</table>

**Top 20 Total**

|         |         |         |             | 52,459 | 53,507 | 2%   |

*Foundry **Fabless

According to IC insights (2013), the top 20 worldwide semiconductor sales leaders for 1Q13 include nine suppliers headquartered in the U.S., four in Japan, three in Europe, and two each in South Korea and Taiwan, a relatively broad representation of geographic regions. Besides, the total sales of semiconductor companies have increased by 2% in 1Q13 as compared to 1Q12. In details, Intel remained at the top position even if their sales decreased by -3%. Moreover, TSMC and Qualcomm had significant increases in the market. With regard to the top five spots, fabless supplier Qualcomm recorded to increase by 28% in sales because it was contributed through the continued success of the smartphone market. Furthermore, top three companies as Intel, Samsung and TSMC have been ranked as same positions. It can be deduced that these companies still have the power of leading semiconductor market.

In addition, IC insights (2013) stated that spending of research and development by semiconductor manufacturers have been increasing for next-generation process technologies. In other words, increasing costs associated with developing complex IC designs has been trended higher for more than three decade.

Figure 6. “Semiconductor R&D Spending 1995-2012”, Source IC insights (2013)

Until 2012, Intel expanded continually spending on new fabs and equipment because their advanced microprocessors and other incredibly complex logic devices have very short life cycles. And then, the amount of spending in Samsung has been declined from 2011. This is because of Samsung still focused on the DRAM and flash memory businesses. Therefore, the main focus of investments is in adding new fab capacity for large-diameter wafers (currently 300mm but heading toward 450mm later this decade, IC insight). In other words, 300 mm wafer system had been well received in the semiconductor manufacturing market. As regarding TSMC, the growth of spending on R&D increased slowly because new generation of ICs has become increasingly difficult to develop.
Consequently, new generation of ICs technologies or larger wafers is required to expand their investment.

Intel, Samsung and TSMC forecasted to expand capital spending on new generation technologies in 2013. In current semiconductor industry, 300mm wafer technology is the prevalent trend of electronic chip manufacturing. In the long term, 300 mm wafer may be inefficient system by increasing demand for cost-effective production. Therefore, these companies will maintain aggressive capital spending plans for a large increase wafers’ capacity and new patterning technologies over the next five years. For example, the next wafer size transition will be 450mm which can optimise the potential per-die cost savings. Besides, the development of EUV lithography for volume production will bring the availability of defect – free mask blanks. A 13.5m wavelength light source of EUV transfers the pattern of the components’ photo-mask onto the wafer’s photoresist substrate engraving or deposition.

<table>
<thead>
<tr>
<th>2013F Rank</th>
<th>Company</th>
<th>2010 ($M)</th>
<th>2011 ($M)</th>
<th>11/10% Change</th>
<th>2012 ($M)</th>
<th>12/11% Change</th>
<th>2013F ($M)</th>
<th>13/12% Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Intel</td>
<td>5,207</td>
<td>10,764</td>
<td>107%</td>
<td>11,000</td>
<td>2%</td>
<td>13,000</td>
<td>18%</td>
</tr>
<tr>
<td>2</td>
<td>Samsung</td>
<td>10,948</td>
<td>11,755</td>
<td>7%</td>
<td>12,225</td>
<td>4%</td>
<td>12,000</td>
<td>-2%</td>
</tr>
<tr>
<td>3</td>
<td>TSMC</td>
<td>5,936</td>
<td>7,333</td>
<td>24%</td>
<td>8,324</td>
<td>14%</td>
<td>9,000</td>
<td>8%</td>
</tr>
<tr>
<td>4</td>
<td>Global Foundries</td>
<td>2,750</td>
<td>5,400</td>
<td>96%</td>
<td>3,000</td>
<td>-44%</td>
<td>3,500</td>
<td>17%</td>
</tr>
<tr>
<td>5</td>
<td>SK Hynix</td>
<td>3,028</td>
<td>3,165</td>
<td>5%</td>
<td>3,655</td>
<td>15%</td>
<td>3,200</td>
<td>-12%</td>
</tr>
<tr>
<td>6</td>
<td>Micron</td>
<td>2,495</td>
<td>2,913</td>
<td>17%</td>
<td>1,773</td>
<td>-39%</td>
<td>2,225</td>
<td>25%</td>
</tr>
<tr>
<td>7</td>
<td>Toshiba</td>
<td>1,762</td>
<td>1,935</td>
<td>10%</td>
<td>1,637</td>
<td>-15%</td>
<td>1,600</td>
<td>-2%</td>
</tr>
<tr>
<td>8</td>
<td>UMC</td>
<td>1,854</td>
<td>1,585</td>
<td>-15%</td>
<td>1,723</td>
<td>9%</td>
<td>1,500</td>
<td>-13%</td>
</tr>
<tr>
<td>9</td>
<td>SanDisk</td>
<td>1,052</td>
<td>1,368</td>
<td>30%</td>
<td>988</td>
<td>-28%</td>
<td>1,000</td>
<td>1%</td>
</tr>
<tr>
<td>10</td>
<td>Sony</td>
<td>460</td>
<td>1,805</td>
<td>292%</td>
<td>1,100</td>
<td>-39%</td>
<td>775</td>
<td>-30%</td>
</tr>
<tr>
<td></td>
<td><strong>Top 10 Total</strong></td>
<td><strong>35,492</strong></td>
<td><strong>48,023</strong></td>
<td><strong>35%</strong></td>
<td><strong>45,425</strong></td>
<td><strong>-5%</strong></td>
<td><strong>47,800</strong></td>
<td><strong>5%</strong></td>
</tr>
<tr>
<td></td>
<td><strong>Others</strong></td>
<td><strong>18,303</strong></td>
<td><strong>18,042</strong></td>
<td><strong>-1%</strong></td>
<td><strong>13,150</strong></td>
<td><strong>-27%</strong></td>
<td><strong>12,035</strong></td>
<td><strong>-8%</strong></td>
</tr>
<tr>
<td></td>
<td><strong>Total Cap Spending</strong></td>
<td><strong>53,795</strong></td>
<td><strong>66,065</strong></td>
<td><strong>23%</strong></td>
<td><strong>58,575</strong></td>
<td><strong>-11%</strong></td>
<td><strong>59,835</strong></td>
<td><strong>2%</strong></td>
</tr>
</tbody>
</table>

According to Intel official website, Intel Corporation was founded by Robert Noyce and Gordon Moore in 1968. Next year, Intel developed the first Metal Oxide Semiconductor (MOS) circuit, the 1101. During this period, the company released the first commercial product which was 3101 Schottky bipolar 64-bit static random access memory (SRAM) chip. However, it was too slow and costly for computer manufacturing. Therefore, the 1103, dynamic random-access memory (DRAM) was introduced in 1970. After that, the Intel 4004 was a 1/8-inch by 1/6-inch chip that contained 2,300 MOS transistors. In other words, it was the first world’s microprocessor with concept of “computer on a chip”. In 1980, the 8080 microprocessor was chosen as the central processing unit of IBM’s first personal computer. Since 1993, the company focused on R&D and manufacturing expertise resulted in the renowned Pentium microprocessor which contributed to make concepts of power performance-intensive applications. In January 2006, Intel had designed the first fully functional SRAM chip using 45-nanometer (nm) logic technology. Following this, the company implemented an innovative combination of materials. For example, it affected to reduce transistor leakage with improving energy efficiency and significantly increasing performance in its 45nm process technology. As a result, the company started to produce the transistor gate in portions of the millions of transistors inside a multi-core computer chip. Moreover, 45-nanometer (nm) processor technology supported to develop with more than 400 million transistors for dual-core processors, more than 800 million for quad-core and the next generation of Intel Core 2.

Intel forecasted that opportunities still exist for cloud and data centre, personal computing, mobile devices and intelligent system in the market (Intel official website). Therefore, the company planned to utilise new generation lithography technologies in their production line. For example, Intel is already using 22nm lithography for manufacturing. Then, the company focused on utilising EUV technology with 13.5nm wavelength. From 2015, Intel will use under 10nm manufacturing process. Consequently, Intel is available to produce high performance microprocessor.

Figure 7. “Intel Manufacturing Technology Road Map”, Source: Intel (2012)
Currently, Intel’s silicon fabs are using both 200mm and 300mm wafers. Two types of wafer still generate stable revenue. However, 200mm wafers will be disappeared, because 300mm wafer has become much more cost effective than a 200mm wafer Fab. After 2015, semiconductor industry expects to release 450mm wafer in marketplace. However, 450mm wafer system requires huge investments roughly $15 billion. Therefore, only 2 or 3 companies in the world will be large enough to have manufacturing sites such as Intel, Samsung and possibly TSMC.

(3) Samsung Electronics Co., Ltd

<table>
<thead>
<tr>
<th>Rank</th>
<th>Company</th>
<th>Market Share (%)</th>
<th>Rank</th>
<th>Company</th>
<th>Market Share (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Samsung Electronics</td>
<td>41.3</td>
<td>1</td>
<td>Samsung Electronics</td>
<td>32.3</td>
</tr>
<tr>
<td>2</td>
<td>Hynix</td>
<td>20.9</td>
<td>2</td>
<td>Toshiba</td>
<td>22.4</td>
</tr>
<tr>
<td>3</td>
<td>Elpida</td>
<td>13.4</td>
<td>3</td>
<td>SanDisk</td>
<td>16.4</td>
</tr>
<tr>
<td>4</td>
<td>Micron</td>
<td>12.1</td>
<td>4</td>
<td>Micron</td>
<td>12.0</td>
</tr>
<tr>
<td>5</td>
<td>Nanya</td>
<td>4.3</td>
<td>5</td>
<td>Hynix</td>
<td>10.3</td>
</tr>
</tbody>
</table>

Table 8. “Market Share in Memory Semiconductor (2010, 4th Q)”, Source: Gartner (2011)

In 1969, Samsung Electronics Co., Ltd was incorporated in the Republic of Korea (Samsung official website). The company has become the world largest memory chip manufacturers with a leading position in the DRAM and NAND flash markets. Currently, Samsung Electronics are challenging Intel’s global market leadership. The company is always required dynamic capability in a dynamic environment. In other words, Samsung Electronics has showed the ability to renew its resource and capability base in response to environmental changes with rapid and flexible responses. Samsung Electronics has developed each generation of DRAM products that experienced the short product life-cycle in marketplace. For example, the competition of DRAM industry requires speed and timing in the memory business. Samsung Electronics represented a variety of methods to compress time for new product development and mass production.

In early years, the company set an aggressive target of completing construction of its fab within six months for the launch of 64K DRAM. In contrast, companies of the U.S. and Japan had normally taken more than 18 months. Besides, Samsung Electronics sought working 24 hours in a crisis mode and in close collaboration with equipment suppliers. As a result, their fab was completed in six months. Moreover, the company established two competing research and development teams for the
development of the 64K DRAM and 256K DRAM in Korea and Silicon Valley of the U.S. Following this, the company focused on R&D effort for mass production of 1M DRAM with its own design and process technologies. In 1986, the 4M DRAM was introduced by collaborating with LG and Hyundai. In this development, Samsung Electronics registered fifty-six patents related to the 4M DRAM and completed the design only six months after Japan (L. Kim, 1997). After that, the company introduced mass production of 16M DRAM in 1990. Then, the company developed continually high performance memory chips such as 64M DRAM in 1992, 256M DRAM in 1994, and 1 Giga DRAM in 1996.

According to Shin and Chang (2006), critical success factors are participation in design and production engineers to all phases of the development process, sharing information and resolving problems quickly by carrying out activities simultaneously rather than sequentially. Besides, the company have spent on aggressive, sustained investment in R&D and production facilities for a leading edge fab. For example, the company decided the risk of investing more than $1 billion in 8-inch diameter wafer processing technology in 1993. Furthermore, it was the first in the industry to move from 6-inch to 8-inch mass production. As a result, their decision have brought significant market share gain and productivity improvement in marketplace. At present Samsung Electronics expanded its market leadership in core businesses, including smartphones and TVs. Moreover, the company decided to invest on ASML’s EUV technology and 450mm wafer system. In other words, it can be another high risk in their development. Nevertheless, it may bring further strengths for the market power of memory business, outpacing competitors with our unmatched technology, dominant cost savings and advanced process technology development.

(4) Taiwan Semiconductor Manufacturing Co. (TSMC)

According to TSMC official website, Taiwan Semiconductor Manufacturing Co. (TSMC) was established in 1987. TSMC has achieved reputation by offering advanced and "More-than-Moore" wafer production processes and unparalleled manufacturing efficiency with leading technologies (TSMC official website). TSMC does not design, manufacture, or market semiconductor products under its own brand name. However, the company provides their microchips to a diverse global customer bases that cover various segments of the computer, communications, consumer, industrial and other electronics market. The company has three advanced fabs such as 12-inch wafer fabs, four 8-inch wafer fabs, and one 6-inch wafer fab. TSMC was the first foundry to provide 65nm and 40nm production capacity. In 2012, the company reached full volume production of 28nm featuring 28HP & 28HPM for high performance and 28LP & 28HPL for low power, and began the initial customer tape out of 20nm technology (TSMC Annual Report, 2012). Furthermore, TSMC supports the general purpose logic process technologies such as DRAM, Mixed Signal/RF, high voltage, CMOS image sensor, MEMS, silicon germanium technologies and automotive service packages. Besides, the
company established its account management and engineering services offices for customer service in North America, Europe, Japan, China, South Korea, and India.

<table>
<thead>
<tr>
<th>TSMC Achievements</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. 0.13μm new generation BCD (Binary Coded Decimal) process for mobile computing is in risk production stage. It offers worldwide competitive power LDMOS Rds(on) performance for better power efficiency and allows micro controller integration to further increase battery life</td>
</tr>
<tr>
<td>2. 90nm uLL (Ultra Low Leakage) eFlash technology qualified and in production for ASIC (Application-Specific Integrated Circuit) and microcontroller applications</td>
</tr>
<tr>
<td>3. 80nm &amp; 0.11μm high voltage process for high resolution HD720 and FHD display driver IC, which could support Retina to Super Retina display quality in smartphones</td>
</tr>
<tr>
<td>4. 65nm joint developed eFlash technology qualified and in production for industrial/automotive microcontroller and smartcard applications</td>
</tr>
<tr>
<td>5. 55nm and 85nm ultra-low power technology for flash controller applications</td>
</tr>
<tr>
<td>6. 55nm &amp; 65nm 5V LDMOS (Laterally Diffused Metal Oxide Semiconductor) for power management application</td>
</tr>
<tr>
<td>7. 55nm low power RF technology for WLAN (Wireless Local Area Network), Bluetooth and other handheld applications</td>
</tr>
<tr>
<td>8. 40nm eFlash for non-volatile memory technologies under joint development for high-end automotive application</td>
</tr>
<tr>
<td>9. 40nm low power and RF technology for smartphones, DTV (Digital Television), STB (Set-Top-Box), game and wireless connectivity applications</td>
</tr>
<tr>
<td>10. 40nm general purpose technology for performance-driven markets like CPU, GPU, FPGA, HDD, Game Console, Network Processor and Gigabit Ethernet applications</td>
</tr>
<tr>
<td>11. 28nm Low Power (28LP &amp; 28HPL) and RF (28HPL-RF) technology for mainstream smartphones, application processors, tablets, home entertainment and digital consumer applications</td>
</tr>
<tr>
<td>12. 28nm High Performance Mobile computing (28HPM) technology for tablets, smartphones, and high-end SoC applications</td>
</tr>
<tr>
<td>13. 28nm High Performance (28HP) technology for performance-driven markets like CPU, GPU, APU, FPGA and high-speed networking applications 20nm System-on-Chip technology (20-SoC) is under development to provide the migration path from 28nm for both performance-driven products and mobile computing applications</td>
</tr>
</tbody>
</table>
14. 16nm FinFET technology (16FF) is under development to provide best value in speed/power optimization to meet next generation products requirements in CPU (Central Processing Unit), GPU (Graphics Processing Unit), APU (Accelerated Processing Unit), FPGA (Field-Programmable Gate Array), Networking and mobile computing applications, including smartphones, tablets and high-end SoC (System-on-Chip) devices


TSMC has shown key differentiating strengths which are technology leadership, manufacturing excellence, and customer trust. Therefore, the company has consistently been recognised the first among pure-play foundries in developing the next generation of leading-edge technologies. For a manufacturing leader, the company utilises yield management to expedite time-to-market and time-to-volume (TSMC official website). Moreover, TSMC’s technology leadership position has been maintained through working on the leading-edge 20nm and 16nm FinFET technologies. For the dual challenges of falling wafer prices and fiercer competition, TSMC seeks continual strengthens with core competitiveness and properly deploys its short-term and long-term technology and business development plans. As regarding short-term semiconductor business development plan, the company is substantially expanding the business and sustain market segment share of advanced technologies with further investment in capacity. Furthermore, TSMC focuses on growing business with Integrated Device Manufacturers (IDMs) by establishing a closer supplier-maker consortium. In the long-term business plan, the company will continually develop the leading edge technologies (EUV technology) with Moore’s law; moreover, the business contribution of “More-than-Moore” will support the development of derivative technology such as 450mm wafer process.

3. Innovation of Next Generation Semiconductor Industry
In the electronic chip production, silicon wafer size is closely related to the economies of scale theory. Each wafer is etched hundreds of memory chips; therefore, larger diameter wafer can produce more electronic chips than small diameter wafers. For several decades, wafer size has shown incremental changes from 25.4 mm (1 inch) to 300 mm (11.8 inches). In other words, wafer size has been affected by incremental changes for cost-effective production. In the current industry, 300mm wafer is the largest size in chip manufacturing; nonetheless, 300mm wafer has limitations of increasing productivity. For this reason, large electronic chip manufacturers invest on the development of 450mm wafer. This chapter will explain how wafer size has changed, and, how the development of 450mm wafer will affect to semiconductor manufacturing.
3-1. Importance of Increasing Silicon Wafer size

(1) History of Changing Wafer size

In semiconductor manufacturing process, a wafer is a thin slice of semiconductor material for using in the fabrication of integrated circuits and other micro-devices. Generally speaking, electronic chip devices still require far smaller, work faster and generate less heat than past devices. Moreover, Moore’s Law is still accepted in the computer industry including the data processing and storage systems. Likewise, the semiconductor industry has experienced an extraordinary revolution in both materials science and in data processing and storage. In current industry, most integrated circuits (ICs) are produced of silicon through using in diameters of 150, 200, and 300mm wafers. For example, each wafer was etched hundreds of memory chips which are developed by the help of computer systems or computer-aided design (CAD) systems. Each size silicon wafers have different capacities to print ICs. For instance, a larger diameters wafer produced more quantity of integrated circuits with more cost effective production; on the other hand, smaller diameter wafer has lower capacity in manufacturing process. For this reason, larger wafers are closely related to the economies of scale theory in electronic chip production.

With respect to semiconductor fabrication, it consists of creating interconnected networks between transistors on the surface of a thin piece of semiconducting material. To put it another way, semiconductors are manufactured on a thin wafer of pure silicon in a facility which is known as a fab. Then, a photolithography process creates transistors on the surface of the wafer, in which successive layers of conducting and insulating materials are deposited on the surface of the wafer and chemically etched away in the appropriate places to form the desired pattern of transistors and necessary interconnections (Byrne D. et al., 2009). In manufacturing progress, each step of the etching process is repeated several times across the wafer for resulting in a grid pattern of many identical copies of the chip.

Silicon wafers have a variety of diameters from 25.4 mm (1 inch) to 300 mm (11.8 inches). According to EE Times (2008), the diameter has gradually increased to improve throughput and reduce cost with the current state-of-the-art fab considered to be 300 mm (12 inch), with the next standard projected to be 450 mm (18 inch). It means that the world semiconductor manufacturing industry requires constantly the demand for faster, more powerful integrated circuits at lower prices. However, increasing productivity by reducing circuitry size would demand cost intensive technologies. When the first full-scale production of integrated circuits began, 3 inches (75mm) of the semiconductor wafers had used to produce electronic chips. Following this, advanced chip production shifted to 4 inches (100mm), to 5 inches(125mm) and then to 6 inches (150mm) by the late 1980s. In this development, technologies of increasing wafer size required significant research and capital investment to ensure reliable production facilities and robust processes. After that, line geometries of
integrated circuits reduced below one micron in the early 1990s. As a result, the semiconductor manufacturing process became even more complex. During this period, the semiconductor industry experienced much more difficulties to move from 6 inches (150mm) to 8 inches (200mm) wafer. Also, semiconductor equipment manufacturers had to change their equipment and systems to adopt consistent quality and repeatability in manufacturing process. And then, the move to 300mm (about 12 inches) allowed manufacturers to produce integrated circuits up to 2.5 times per wafer rather than 8 inches (200mm) wafer. Likewise, semiconductor fabrication technology has shown discrete steps about wafer size and line width. For example, large numbers of chips on a given wafer can be produced by increasing in wafer size. Currently, most fabs offer 150mm, 200mm, or 300mm diameter wafers. According to (Kumar, 2007), for representative line widths and die size, the move to a larger wafer has generally resulted in overall savings of approximately 30% per die. In other words, a larger diameters wafer is able to fit many more die of a given size, even if larger wafers require more costs to produce. Consequently, increasing space on a wafer is necessary to achieve the appropriate cost-per-chip ratio in the near future.

<table>
<thead>
<tr>
<th>Wafer Size (inch)</th>
<th>Wafer Size (mm)</th>
<th>Thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-inch</td>
<td>25 mm</td>
<td>-</td>
</tr>
<tr>
<td>2-inch</td>
<td>51 mm</td>
<td>275 µm</td>
</tr>
<tr>
<td>3-inch</td>
<td>76 mm</td>
<td>375 µm</td>
</tr>
<tr>
<td>4-inch</td>
<td>100 mm</td>
<td>525 µm</td>
</tr>
<tr>
<td>5-inch</td>
<td>130 mm or 125 mm</td>
<td>625 µm</td>
</tr>
<tr>
<td>6 inch</td>
<td>150 mm</td>
<td>675 µm</td>
</tr>
<tr>
<td>8 inch</td>
<td>200 mm</td>
<td>725 µm</td>
</tr>
<tr>
<td>12 inch</td>
<td>300 mm</td>
<td>775 µm</td>
</tr>
<tr>
<td>18 inch</td>
<td>450 mm</td>
<td>925 µm (expected)</td>
</tr>
</tbody>
</table>


In the semiconductor industry, wafer size with new fab architecture has increased roughly every ten years while technology is advanced every 2 years. An increase of wafer size becomes more critical as technology advanced getting slower due to the physical limitations involved in nanotechnologies (Chien et al., 2007). Moreover, new wafer size platforms improved the incorporation of semiconductor equipment suppliers and IC makers for advanced process technologies and tool designs. Indeed, the move from 150mm to 200mm took about 7 years. In contrast, it took over 10 years from 200mm to 300mm. Though, larger wafer size requires the significant capital investment to create entry barrier, wafer size enlargement is inevitable to maintain industry growth and vertical collaborations.
During the past four decades, Moore’s Law has suggested as a remarkable guide to the dynamics of the silicon based electronics revolution. It showed the significant technological development and advanced manufacturing productivity. Furthermore, Moore’s Law is based on an economic law that one technology generation to the next technical performance has contributed to a 30% cost savings. Thus, the cost reduction of semiconductor manufacturing process allows firms to provide increasingly innovative products to customers at lower prices. According to PWC Technology Institute (2014), factors of semiconductor manufacturing such as wafer size transitions and improving equipment productivity contributed to the improvements in productivity and reduction in cost as the annual 25%-30% productivity gain.

(2) New opportunity of 450mm Wafer

The demand for never-ending reduction in bit cost brought the accelerating development of semiconductor devices and production technology. A core of the International Technology Roadmap of Semiconductors (ITRS) is affected by Moore’s law that suggested a technology target for the semiconductor industry. According to ITRS, 450mm wafer will be the next generation wafer size. In the last generation, the implementation of 300mm wafers from the 200mm showed a 30% cost reduction. The 450mm wafer transition creates new opportunity to implement another wave of innovations on equipment performance. Therefore, process control, productivity, manufacturing system and improvements in uniformity have to be required for cost benefits. Currently, the semiconductor industry has an experience of development the 300mm wafer. In other words, the industry forecasts a reality, sustainable and cost-effective of larger diameter wafers:
For the next wafer size transition, machinery will be required to handle and process larger wafers results in increased investment costs to build a single factory. Historically, the worldwide capacity of 300m wafer process just accounted for roughly 20% in 2005. This is because the step up to 300mm needed fully automated factories with high cost rather than 200mm wafers. However, the demand for 300mm wafer becomes to have approximately 60% of wafer market in 2014. Therefore, it can be seen that significant engineering, time and cost to overcome are required for the development of 450mm wafers. After that, the factory architecture of 450mm wafer process will be adaptable across all business models in IC manufacturing including DRAM, high mix logic, foundry and high volume microprocessors.

<table>
<thead>
<tr>
<th>Wafer diameter</th>
<th>300mm wafer</th>
<th>450mm wafer</th>
</tr>
</thead>
<tbody>
<tr>
<td>An area of wafer</td>
<td>70,685mm²</td>
<td>159,043mm²</td>
</tr>
</tbody>
</table>

Installed Capacity Leaders per Wafer Size as of Dec-2013
(Ranked by Share of Total WW Installed Monthly Capacity)

<table>
<thead>
<tr>
<th>300mm Wafer</th>
<th>200mm Wafer</th>
<th>150mm Wafer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Samsung</td>
<td>TSMC</td>
<td>STMicro</td>
</tr>
<tr>
<td>Micron</td>
<td>Texas Instruments</td>
<td>CR Micro</td>
</tr>
<tr>
<td>Toshiba/ SanDisk</td>
<td>UMC</td>
<td>Renesas</td>
</tr>
<tr>
<td>SK Hynix</td>
<td>Infineon</td>
<td>Panasonic</td>
</tr>
<tr>
<td>TSMC</td>
<td>Samsung</td>
<td>ON Semi/Sanyo</td>
</tr>
<tr>
<td>Intel</td>
<td>Renesas</td>
<td>Silan Micro</td>
</tr>
<tr>
<td>GlobalFoundries</td>
<td>STMicro</td>
<td>TSMC</td>
</tr>
<tr>
<td>UMC</td>
<td>GlobalFoundries</td>
<td>Rohm/Lapis</td>
</tr>
<tr>
<td>Powerchip</td>
<td>Toshiba</td>
<td>Toshiba</td>
</tr>
<tr>
<td>Nanya</td>
<td>Huahong Grace</td>
<td>KEC</td>
</tr>
</tbody>
</table>


As the requirement of huge investment in 450mm process, only large semiconductor manufacturers decided to install cutting-edge production facilities. According to Intel (2008), Intel Corporation, Samsung Electronics and TSMC agreed the need for industry-wide collaboration to target a transition to larger, 450mm-sized wafers. Then, these companies also explained that the transition to larger wafers will bring continued growth of the semiconductor industry and helps maintain a reasonable cost structure for future integrated circuit manufacturing. Based on historical production wafer development, manufacturing with larger wafers improves the ability to produce semiconductors at a
lower cost. For example, 450mm wafer is one and a half times larger than 300mm wafer; however, the number of printed die (individual chips) will be more than twice. In other words, the larger wafers help lower the production cost per chip. Moreover, larger wafers will help diminish overall use of resources such as more efficient use of energy, water and other resources.

![Figure 9. “Historic and projected semiconductor demand by wafer size”, Source: IC knowledge](image)

Nonetheless, the complexity of advanced technology is still a concern to increase cost for the future. Intel Corporation, Samsung Electronics and TSMC try to apply aligned standards, rationalizing changes from 300mm infrastructure and automation that will reduce 450mm research and development costs. The cooperation between those companies will support to minimise risks and transition costs with a potential solution to maintain a reasonable cost structure for the industry.

(3) Economics of 450mm Wafer System

In the semiconductor industry, the economic situation is the most important concern. Historically, silicon suppliers have improved new technologies to meet industry demand and competitiveness in the market. However, the 450mm wafer case can be different. The largest economic factor can affect to the production of 450mm wafers with economics driven and fab cost. In other words, the expected R&D cost of developing a 450 mm wafer pilot production fab will be large by different poly silicon usage and wafer shaping etc. For this reason, some silicon suppliers may hesitate to start 450 mm R&D. For successful migration of new wafer size platform, collaborations of the supply chain from upstream suppliers are required by introducing new equipment, silicon wafer, wafer carrier, testing house and factory automation to downstream chip maker. Nevertheless, high fab capital requirement can be advantage in the semiconductor market with the barriers for new entrants in either suppliers or makers side. Consequently, the market structure will show duopoly market, even though the 450mm wafer generation introduction will increase the switching cost. Additionally, memory market segment will be also changed by the adoption of the 450mm wafer size. For example, memory die sizes have been continually reduced through increasingly capable of profitably scaling to lower technology
nodes. Thus, if companies who accept uncertainty and plan for the transition from both product
development and operations perspectives, it will help to reduce die costs and increase market share.

In the long term, the cost of 450mm process can be stable by increasing wafer productivity and
closely supplier-maker consortium cooperation and collaboration. According to Chien et al. (2007),
the back-end (Testing and Assembly) suppliers and makers should also synchronize respective cost
reduction for overall industry improvements, such as wafer-level package technology. The
semiconductor industry expects that cost pressure will usually pass upward to suppliers. Therefore,
the migration of 450mm wafer is a strategic decision for the whole industry. Besides, the existing
competition and threat of new entrants will be continued for keeping market competition in this
industry. However, effectiveness of the next wafer size transition can be dynamically and interactively
influenced by many sectors of supply chain. For example, there are two types of buyers such as
commodity buyers for low cost solutions and value buyers from diversified new semiconductor
applications. Consumers and value product will consistently require high-mix and low-volume for
profitability. On the contrary, the commoditised market and shorter product life can cause revenue
growth slower under mature semiconductor manufacturing industry.

3-2. Extreme Ultraviolet (EUV) Technology Development
The photolithography technology is a key process of manufacturing integrated circuits (ICs).
Moreover, shorter wavelengths can produce high performance ICs. In the current lithography industry,
most fabrication tools use "deep ultraviolet (DUV)" spectrum with wavelength of 193nm. The next
generation technology is EUVL which use “laser-produced plasma” (LPP) with wavelength of 13.5
nm. Therefore, EUVL can produce higher performance ICs with using delicate printing or patterning.
In other words, EUVL will be the disruptive technology in the semiconductor equipment market. As
we shown in Chapter 1, radical innovation can cause some disadvantages such as high risks and a large amount of investment on R&D with a highly uncertain return on investment. Nevertheless, ASML’s challenge will be a significant strength as a first-mover in the semiconductor equipment market. As a consequence, this chapter will discuss why the development of EUVL is radical innovation and how ASML has the monopolistic position.

(1) Development of EUV

During the last several decades, optical projection lithography has become an important lithography technique for the high-volume manufacture of integrated circuits (ICs). Photolithography is a critical process for manufacturing ICs which is key internal semiconductor components such as patterning and IC layout on a silicon wafer. For example, photolithography mainly consists of three parts: the pattern printer, photoresist technology and the mask fabrication. In the previous generation, most lithography machines utilised light in the "deep ultraviolet (DUV)" spectrum. On the contrary, extreme ultraviolet (EUV) is the light source that is used for next generation technology. EUV has a shorter wavelength than visible light with a wavelength of 10 to 14 nanometres (nm) which sits in the spectrum between visible light and X-ray. Currently, semiconductor manufacturers continually seek a shorter wavelength in the chip manufacturing. In other words, Extreme Ultraviolet Lithography (EUVL) is a relatively new form of next-generation photolithography.

With respect to the changes of photolithography, the semiconductor industry introduced lithography technology when ICs were invented in 1958. In the early development, light of the visible g-line (436 nm) and the ultraviolet i-line (365 nm) were used with a mercury arc lamp. And then, the semiconductor equipment industry needed to reduce the feature size for manufacturing high performance ICs. Once deep ultraviolet 248 nm krypton fluoride laser (KrF) and 193 nm argon fluoride laser (ArF) were introduced, the g-line and i-line disappeared in the semiconductor industry. Likewise, the Next Generation Lithography (NGL) is continually studied in order to produce IC with shorter wavelength.

In 1988, soft X-ray projection lithography was proposed, nonetheless, the wavelength range of EUV and soft X-ray was not clearly defined until early 1990s. In the early and mid-1990s, the Lawrence Livermore National Laboratory (LLNL), Sandia National Laboratory (SNL), and Lawrence Berkeley National Laboratory (LBNL), as well as AT&T Bell Laboratories and several universities mainly performed systematic research of EUVL (Wu, B. & Kumar, A., 2009). After that, Intel, Motorola, and Advanced Micro Device (AMD) continued work on EUVL among an industrial consortium. During this period, the Extreme Ultraviolet Concept Lithography Development System (EUCLIDES) of Europe was formed in 1998 by ASML Carl Zeiss, and Oxford Instruments. Following this, EUVL studies with ASML leading have made significant progress. In Japan, NTT Large-Scale Integration (LSI) Laboratories were performed for EUVL studies in 1989. Then, other EUVL pioneers such as Nikon and Hitachi also started their EUVL research since 1990. In 2002, Japan established the Extreme Ultraviolet Lithography System Development Association (EUVA) which helped to improve technologies of new generation lithography. Currently, EUVL researches are being mainly conducted by industrial consortiums and companies such as SEMATECH, IMEC, ASML, Global foundry, Intel, Samsung, TSMC, Toshiba, Hynix, and IBM.

(2) Benefits of EUV Technology

It is possible to argue that the entire semiconductor industry requires packing transistors more tightly with shrinking the size of transistors. When the semiconductor equipment industry accepted an optical technology, it showed a limit to improve resolution of the equipment with the wavelength of the light. In other words, higher resolution and smaller features come from shortening the wavelength of the light. In the early photolithography industry, most machines used ultraviolet light with a wavelength of 365 nanometres to DUV light of 248 nanometres and 193 nanometres. Therefore, EUV is another disruptive lithography technology with using light of a wavelength of 13.5 nanometres. In addition, DUV utilises Arf laser process, on the other hand, EUV light source has two ways such as “Laser-Produced Plasma” (LPP) and “Discharge Produced Plasma” (DPP) sources.
Using DUV lithography has another limitation. If DUV lithography for shorter wavelength of light will use to absorb the condenser glass lens, the light source cannot reach or generate any pattern on the silicon wafer. However, the glass lens of EUV lithography will be replaced in order for the condenser mirror system.
The current EUV lithography uses a laser plasma source with a wavelength of 13.5nm. The laser plasma source of work in a vacuum environment produces extreme ultraviolet rays. In details, heated xenon gas produces plasma, then, it begins to escape through sending the light of a wavelength of 13.5nm. And then, the plasma will light and shine on the mask. For example, mask pattern is reflected to the four to six curved mirrors. Therefore, the image thumbnail, and image put into the silicon wafer together; each slightly curved mirror to light to form images on the wafer, it is like the camera in the lens to bend light to form an image on film the same (Semi, 2011). During the entire process, it must be conducted in a vacuum. Besides, molybdenum and silicon of EUV process coated with layers of concave and convex mirror. Therefore, a reflection coating would be nearly 70% of the wavelength of 13.5nm extreme ultraviolet light, and the other 30% were mirror absorption. If there is no coating, the light before reaching the wafer will be almost completely absorbed (Semi, 2011). In other words, it must be almost perfect mirror, even small defects in the coating will also damage the shape and distortion of the optical circuit design, leading chip functionality problem. As EUVL using short wavelength light for imaging, the mirrors have to be required to exhibit an unprecedented degree of perfection in surface figure and surface finish for diffraction limited imaging. Consequently, for the demand for the printing of ever smaller features, lithography equipment manufacturers have developed to gradually reduce the wavelength of the light used for imaging and to design imaging systems. In other words, EUV technology is different form rather than the visible and UV ranges.

(3) Challenges of ASML

According to ASML official website, ASML has already spent as much R&D expenditure on the previous two generations (ArF dry and ArF immersion) combined. It is clear that using a "laser-produced plasma" (LPP) source for EUV technology are difficult to produce. In other words, a high-energy laser fires on a microscopic droplet of molten tin and turns it into plasma, emitting EUV light,
which then is focused into a beam (ASML, 2014). Nonetheless, chip makers will have the benefits of EUVL. For example, the current problems of photolithography technology have come at the cost of increasing complexity and shrinking margins of error. Furthermore, the semiconductor equipment industry still has to reach deep into a bag of tricks to continue shrinking feature sizes. If electronic chip makers have to use double patterning technology with DUV for shorter wavelength, the cost of lithography exposures per wafer would be increased by inefficient fab output and requiring more equipment. However, chip manufacturers with EUVL just need to expose a critical layer in just one single step with a resolution of less than 10 nanometres. According to Taiwan ASML's Strategic Marketing Director Peter Cheang, EUV technology uses wavelengths over the existing lithography equipment reduced by more than 10 times, make the future 10nm technology nodes to achieve even smaller (ASML official website). To put it another way, the benefits of EUVL will continue to support the advance of Moore's Law.

In the current semiconductor industry, ASML is the first mover to the next generation lithography technology. Moreover, it is true that the first mover with next generation technology always requires huge R&D investment and infrastructure issues. The early EUV production tools of ASML named the NXE: 3300 produces 69 wafers an hour (ASML official website). In other words, their EUV equipment has not shown proper cost effectiveness in marketplace. It means that some chip manufacturers are still hesitating to purchase EUV equipment. In the chip manufacturing, lower cost per wafer and higher throughput are key factors to move to the next generation technology.

![EUV Cost/Mpixel ($) at Different Resolution and Throughputs](image)

Figure 14. ‘Projected EUV Cost/pixel at Different Resolutions and Throughputs’ Source: Preil (2012)
Indeed, the semiconductor industry requires throughputs of around 100 wafers an hour to make EUV economically viable in production fabs. Therefore, ASML is still developing to deliver EUV tools with a stable performance. For example, EUV process has increased possible shrinkage and production yields; moreover, cycle time is still reduced at the expense of non-lithography process steps. Furthermore, ASML showed that EUV lithography can reduce cycle times by 30% compared to double patterning and up to 75% compared to spacer defined quadruple patterning (ABN AMRO Bank, 2013). In other words, the number of non-lithography process steps will be significantly decreased by developing critical layers with a single exposure. Consequently, a lower cycle time will bring lower costs per chip through increasing the output of a fab. Since, ASML has made significant progress on its EUV roadmap, the company expected that it can roll-out 60-66 EUV machines in 2016 (ABN AMRO Bank, 2013).

(4) Expectation of EUV Technology Development

Electronic chip market has been requiring both the exponential cost reduction per component and the exponential shrinkage of the component size on the chip. The current technology is still based on the 193nm wavelength immersion technology. The EUVL uses 13.5nm wavelength. Therefore, the dramatic decrease in wavelength will bring a straightforward gain market shares in the semiconductor equipment market. ASML is continually trying to develop the industry’s technology shrinks such as integrating computational lithography, wafer lithography and process control. In recent year, ASML have introduced NXE scanner platform and of generic EUV effects. Therefore, ASML’s customers will be available to utilise the EUV lithography on their IC-devices and speed up their learning cycles in the semiconductor factories.

By introducing EUVL, ASML expects three scenarios for EUV adaption dependent on throughput: (ASML official website)

1) Clients will only adapt EUV for a limited number of layers (1 or 2) and get a scaling benefit of 1.7-1.8x compared to 1.5x with multiple patterning.
2) Clients will adapt EUV for 5-7 layers and get a scaling benefit of 2.0x.
3) Clients will use EUV for up to 17 layers.

The semiconductor manufacturers will accept EUVL machines. With a throughput of 70 wafers per hour, the semiconductor equipment industry will adapt the technology of 5-7 layers at 10nm logic nodes. Therefore, ASML forecasted this technology will bring 60-66 EUV machines being sold in 2016 with an average selling price of EUR 80-100m. That is, EUV revenue may reach up to UR 4.8-6.6bn in 2016.
Once ASML introduced the EUV tools (NXE: 3300B), it showed a throughput at 69 wafers an hour. The semiconductor manufacturers still require ‘stable performance’ productivity with maximum throughputs 125 wafers an hour. According to ASML’s roadmap, the company has assumptions that next generation of EUV machine will show to extend the source power in order to increase throughput further (ASML official website). The development of EUV needs to spend huge amount of R&D expenditure. As such, high volume manufacturers such as Intel, Samsung and TSMC agreed to invest monopolistically in ASML’s next generation technology. In other words, the co-investors have taken the risk of losing market competitiveness if EUV technology will be delayed in the semiconductor equipment market. Nevertheless, the investors expected that new technology will have experiences of the availability of alternative techniques, potential cost savings for clients and the economic state of the world.

Currently, ASML has the second largest market share in the semiconductor equipment market (ASML official website). Besides, the EUV acceptance has grown gradually with the expectation of superior production yields for next generation chips. For example, EUVL will make a significant reduction in the number of non-lithography process steps through developing critical layers with a single exposure. In addition, both SEMI (2014) and Gartner (2014) expected positively the entire semi equipment spending as a result of a strong rebound in memory spending. ASML believed that investors will focus on EUV upside with clients’ capital expenditure programmes. Furthermore, ASML has six pre-production EUV development tools in the field; however, these tools lack the throughput required for economical chip production in high volume. Consequently, ASML will have the monopolistic position in the semiconductor equipment market.
4. Management of Innovation at ASML

As we shown Chapter 3, the development of EUV technology requires an increase of investment on R&D. For this reason, ASML has introduced new management of innovation called “Customer Co-Investment Programme (CCIP)”. It will accelerate the development of EUVL and future 450mm silicon wafer system. In this programme, Intel Corporation, Samsung Electronics and TSMC agreed R&D funding commitments. Therefore, the CCIP can be either risk sharing or “win-win” strategies. In this Chapter, we will discuss the details and effects of the CCIP with the three customers.

4.1. New Funding Programme of ASML

(1) Customer Co-Investment Programme (CCIP)

To deliver smaller, faster, cheaper and lower power devices cause to increase manufacturing complexity and capital expenditures. Moore’s Law stipulated that transistor density and microchip performance doubles roughly every 18 months. However, the Moore’s Law requires significant increasing investments by both the semiconductor manufacturing and the semiconductor equipment industry. Therefore, ASML decided to launch new innovative investment programme to develop next generation technologies. In other words, the funding programme by a leading semiconductor manufacturer an acknowledgement of the essential contribution of lithography technology in ensuring the continuation of Moore’s Law (ASML, 2013). In 2012, ASML introduced their Customer Co-Investment Programme (CCIP) to accelerate the development of EUVL and future 450mm silicon wafer technology. In this funding programme, ASML needed to receive as the target for aggregate R&D funding commitments of EUR 1.38 billion. Thus, it can be deduced that the CCIP creates risk sharing with the largest customers such as Intel Corporation, Samsung Electronics and TSMC. ASML Chief Executive Officer Eric Meurice said the investment program is a “win-win,” giving ASML funding and allowing the shareholders to benefit from a possible appreciation in the company’s value. Furthermore, R&D investments will be resulting in substantial manufacturing productivity gains, product power and performance enhancements.

According to ASML (2013), the customers collectively agreed to fund EUR 1.38 billion of ASML’s research and development projects from 2013 to 2017. Besides, the funding commitments that the Participating Customers agreed to invested in ordinary shares equal, in aggregate, to 23 percent (EUR 3.85 billion ) of ASML’s issued share capital (ASML, 2013).

Even though, ASML’s customers purchased by 23% shares, the customer co-investment program have no effect on the total current number of ASML shares outstanding. In other words, the aggregate subscription comes from the First Issuance and the Second Issuance. Therefore, a synthetic buy-back consists of a repayment to shareholders of the aggregate subscription proceeds and a reverse stock split. These shares have non-voting, except in limited extraordinary circumstances. Thus, the CCIP will maintain ASML’s strategic and operational independence.

4-2. Details of Co-Investors’ Participations

(1) Intel Corporation

It is clear that Intel Corporation is the largest co-investors of ASML. In details, Intel agreed to invest €829 million in ASML’s R&D programs for EUV and 450mm wafer deployment, to purchase €2.5 billion worth of ASML shares (ASML official website). In other words, Intel showed a multi-party development programme that includes a cash contribution and equity investments. It is possible to say that Intel’s participation will result in significant cost savings and other productivity improvements for semiconductor manufacturers. Brian Krzanich (Intel senior vice president and chief operating officer) said that "Productivity improvements driven by enhanced wafer manufacturing technologies, especially larger silicon wafers and enhanced lithography technologies with EUV are direct enablers of Moore's Law, which delivers significant economic benefits to consumers" (Intel official website).

With respect to risk factors, Intel recognised that risks and uncertainties may arise from difficulties or delays in research and development of 450-mm and EUVL technologies. For example, pricing pressures and actions taken by competitors may come from the timing and execution of the manufacturing ramp and manufacturing yields. Nonetheless, it is true that Intel needs to keep on pace
with Moore's Law. For instance, larger 450-mm wafers and EUVL will offer the benefit of productivity improvements with a 30 to 40 percent reduction in die cost.

(2) Samsung Electronics

Samsung Electronics decided to join ASML’s CCIP for innovation and R&D. The company contributed EUR 276 million for next generation lithography technologies. Moreover, Samsung has committed to invest EUR 503 million in a 3 percent ASML equity stake under the same general terms as the other co-investors. Samsung Electronics is the world second largest chip manufacturer and the company needs to meet worldwide demand with manufacturing capacity utilization for their customers including the impact of general economic conditions on consumer confidence. Following this, the continuing success of technology advances will affect to new product development and customer acceptance of new products. For example, the development of EUV technology will reduce the ICS’ pattern and size of chips with increasing their capacity and speed for devices such as mobile phones and tablet computers. Consequently, the investment decision of Samsung Electronics will be “a win-win” strategy to keep their market position (Samsung official website).

(1) Taiwan Semiconductor Manufacturing Co. (TSMC)

Taiwan Semiconductor Manufacturing Co. (TSMC) has joined the CCIP of ASML to invest EUR 276 million in research and development of next generation lithography technologies and as EUR 838 million in a 5 percent ASML equity stake. By this decision, TSMC expected that the R&D contribution will support secure EUVL development activities and speed up the deployment of new technologies for 450 mm wafer system. Shang-yi Chiang (TSMC executive vice president and co-chief operating officer) mentioned that "We are confident that the additional funding for ASML's research and development programs will help the industry control wafer cost, and therefore protect the economic viability of Moore's Law" (TSMC official website). Furthermore, TSMC estimated that if the R&D programmes progress satisfactorily as expected, the company would migrate to 450mm wafer technology in 2014. Furthermore, the process of photographically printing semiconductor designs with EUVL will remove even small defects in the photolithography process.
5. Strategic Management of Semiconductor Equipment Industry

For market competitiveness, companies need to find both aggressive and defensive strategies. In recent year, the semiconductor equipment market has experiences of two significant merger and acquisition. ASML merged Cymer who has unique laser knowledge of semiconductor photolithography. Therefore, this merger will support to improve the development of EUVL technology. Besides, Applied Materials decided to merge Tokyo Electron. These two companies already have the largest market share. In other words, this merger will be a defensive strategy against accelerating EUV technology of ASML. This chapter will explain how their M&A affects to the structure of semiconductor equipment market.

5-1. ASML’s Merger Agreements with Cymer

Cymer, Inc. is an industry leader in developing lithography light sources. Currently, the innovations of Cymer are pioneering the industry's transition to EUV lithography. In 1986, Cymer was founded by Dr. Robert Akins and Dr. Richard Sandstrom (Cymer official website). The company applied their unique laser knowledge of semiconductor photolithography to the personal computer market. In the mid-1990s, the company introduced light sources as a necessary component in the development of advanced semiconductor tools. This is because of increasing the demand for light sources in the semiconductor equipment market. By the end of 2000s, Cymer sold shipped more than 3,300 KrF (248 nm) and ArF(193 nm) and ArF Immersion light sources world-wide. In 2005, a joint venture between Cymer, Inc. and Carl Zeiss SMT AG was formed to develop a manufacture a silicon crystallization process tool for use in the production of flat panel displays and OLED displays (Cymer official website). In 2012, ASML announced that they would acquire Cymer for their EUVL equipment strategy. In other words, the merger aims to accelerate the development of EUV technology through working with Cymer’s light source technologies.

EUVL uses a 15 times shorter wavelength than DUVL systems that enables semiconductor scaling to resolutions of 10(nm) and smaller. For example, Bob Akins, chief executive officer of Cymer explained that chips patterned by EUV lithography will be hundreds of times more powerful than today's. Therefore, light source technologies of Cymer are a key piece of ASML’s next generation systems.

The EUVL system require higher power light source with large amount of investment on R&D for cost-effective and high-performance chip manufacturing. For this reason, perfecting the lasers may be
taken longer than expected by other less efficient manufacturing techniques. For instance, the current ASML’s product (NXE:3300B) has a throughput at 69 wafers an hour with 105 watts light power. For mass production of wafers, ASML needs to boost power levels to 250 watts of power. Following this, the EULV products will show more than 100 wafers throughput per hour when fully integrated into ASML scanners.

Consequently, the merger will make the significant EUV technology development with more efficient and integration flow of the EUV modules. In addition, the transaction also includes Cymer’s DUV business. As a result, ASML and Cymer can continue to deliver DUV and EUV sources for all semiconductor manufacturers (Cymer official website). Moreover, the merger helps to cooperate closely with streamlining project management and simplifying the supply chain for a number of development tasks. Therefore, it can be seen that the risk of moving to extremely complex technology can be reduced through combining Cymer’s expertise in EUV light sources with ASML’s expertise in lithography systems design and integration.


For a defensive strategy, companies often try to find merger and acquisition opportunities when R&D costs are going up and the number of customers is going down. In the semiconductor equipment market, Applied Materials Inc. and Tokyo Electron Ltd., these two companies have shown the largest market share (Applied Materials official website). In 2013, Applied Materials agreed to buy Tokyo Electron for $9.39 billion. This agreement will show deals to build on the combined company’s share of the market for electronic chip-making equipment. The companies expected that the transaction will be completed by the second half of 2014. According to Amano, T. and Womack, B. (2013), the integration of two companies will bring about 25 percent of the global market. Therefore, this merger and acquisition will be threat to other competitors such as ASML, Lam Research and KLA-Tencor.

In details, most electronic chip manufacturers need to boost high-performance, lower-power and Micro-Electro-Mechanical (MEM) chips. In addition, Gartner (2013) stated that spending on semiconductor equipment by the top five chipmakers will make up more than 65 percent of total 2013 spending. It means that most companies are moving to next generation technologies such as EUVL and 450mm wafer system. In other words, Applied Materials and Tokyo Electron produce semiconductor machines that prepare silicon wafers for imprinting with the circuits that turn them into processors capable of crunching numbers and connecting to mobile networks etc. As a consequence, a combined Applied Materials and Tokyo Electron will be better navigation an industry under pressure as lower costs and high performance devices.
### Market shares of IC manufacturing equipment market

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<th>Pre-merger</th>
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<td>2. ASML: US$ 4.9 billion (12.8%)</td>
<td>2. ASML: US$ 4.9 billion (12.8%)</td>
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<td>3. Tokyo Electron: US$ 4.2 billion (11.1%)</td>
<td>3. Lam Research: US$ 2.8 billion (7.4%)</td>
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<td>4. Lam Research: US$ 2.8 billion (7.4%)</td>
<td>4. KLA-Tencor: US$ 2.5 billion (6.5%)</td>
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<td>5. KLA-Tencor: US$ 2.5 billion (6.5%)</td>
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Before combining Applied Materials and Tokyo Electron, Applied Materials had 14.4% of market share in the semiconductor equipment market. Moreover, Tokyo Electron was third largest company with 11.1% of market share in this industry. After merger, these companies will have 25.5% market share. Besides, their combination will enable to adapt the technology better and be the lowest-cost supplier with the development of complementary products. Therefore, this merger can be seen as a defensive strategy against accelerating EUV technology of ASML.
6. Conclusion

To sum up, it is clear that firms seek to find strategic innovation when they faced limits in the market competition. Innovation can introduce new technological developments and significant systemic changes in many industry areas. If a firm decided to develop any innovation, the firm may take considerable risks in their processes. Nevertheless, innovation may lead to move to next generation waves with dramatic improvements. As we shown in innovation theory chapter, there are two types of innovations which are incremental and radical innovation. Incremental innovation usually uses existing technologies and process. On the contrary, radical innovation seeks significant changes through developing disruptive technologies and processes for future improvement. In other words, incremental innovation has approaches to continuous improvement with low risks. However, radical innovation can destroy the existing markets through technological breakthroughs. For this reason, it requires large amount of investment on R&D with a highly uncertain return on investment. Nonetheless, radical innovation has benefit as the first mover with market strengths. For example, if a company shows successful radical innovation, they will be in a monopolistic position with related profits.

In semiconductor industry, the development of Integrated circuit(IC) has affected the trend of global electronics industry. The technology of ICs has been based on “Moore’s Law” that the number of components per chip would increase a doubling every 18 months (changed to “a doubling every two years”). For the last century, ICs has shown significant improvements such as high performance and low power electronic chips with mass production system. Therefore, the demand for semiconductor tools has also increased by electronic chip manufacturers. In the current semiconductor equipment industry, manufacturers focus on next generation technologies such as 450mm wafer system and EUV technology. For example, 450mm wafer will be the next generation wafer size. The development of 450mm wafer affects to improve productivity of fab equipment with economies of scale production. For example, it will be is one and a half times larger than 300mm wafer, however; the number of printed die (individual chips) will be more than twice. Besides, Extreme Ultraviolet lithography (EUVL) will be the new generation wave of photolithography. As regarding the photolithography technology, a shorter wavelength enables to reduce the feature size for manufacturing high performance ICs. In the previous generation, most photolithography machines have been using light in the "deep ultraviolet (DUV)" spectrum with a wavelength of 193nm. EUVL will introduce a shorter wavelength than visible light with the wavelength of 10 to 14 nanometres (nm). In other words, higher resolutions and smaller features will come from shortening the wavelength of the light source. Consequently, it can be deduced that wafer size has been affected by incremental changes for cost-effective production. In contrast, the development of EUVL is radical innovation with technological breakthroughs of photolithography.
It is clear that incremental and radical innovation are fundamental approaches to accept new technological trajectory. However, it requires spending huge amounts of R&D expenditure. It means that some companies may hesitate to invest in next generation technologies both 450mm wafer system and EUV technology. Nevertheless, ASML accepted new challenges to develop next generation technologies. For financial requirement, the company introduced Customer Co-Investment Programme (CCIP) with their large customers such as Intel Corporation, Samsung Electronics and TSMC. In other words, the CCIP is risk sharing and “win-win” strategies for both semiconductor equipment and electronic chip manufacturers. Thus, ASML decided to introduce their radical changes in the semiconductor equipment industry. ASML’s strategic decision will be as a first mover to develop the next generation photolithography. Even though, the company has taken the high level of risk and high cost of failure, ASML will have the monopolistic position in the semiconductor equipment market.

In addition, the industry has experienced both aggressive and defensive strategic management. For example, ASML announced to acquire Cymer Inc. for their EUV equipment strategy. This is because of Cymer has unique laser knowledge of semiconductor photolithography. Therefore, the merger will be a key piece of ASML’s next generation systems. In the semiconductor equipment market, Applied Materials Inc. showed a defensive strategy. The company decided to merge Tokyo Electron Ltd. in 2013. This merger has brought the largest market share to Applied Materials in the semiconductor equipment market. As a consequence, a combined Applied Materials and Tokyo Electron will be a threat to other competitors such as ASML, Lam Research and KLA-Tencor.

In 2014, ASML has released NXE: 3300B which used 13.5nm and 105 watts EUV light source with 69 wafers production throughout per hours. However, the electronic chip manufacturers till require ‘stable performance’ productivity with maximum throughputs 125 wafers an hour. For increasing productivity, EUV tools need to boost power levels to 250 watts of power. According to ASML’s roadmap, the company expects that EUV machine will show to increase the source power in order to increase throughput. Furthermore, EUVL will make a significant reduction in the number of non-lithography process steps through developing critical layers with a single exposure. With respect to develop 450mm wafer, this system will be introduced in electronic chip production after several years. Following this, the market segment of electronic memory will be also changed by the adoption of the 450mm wafer size with increasing productivity. After that, 450mm wafer process will be adaptable across all business models in IC manufacturing including DRAM, high mix logic, foundry and high volume microprocessors. Likewise, incremental and radical innovation plays an important role in the semiconductor equipment industry. The development of 450mm wafer system and EUV technology is not destination for its industry. The market demand for faster and smaller features electronic products will affect to create new innovative technologies in the future.
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